(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 831 625 A2

(12) **EUROPEAN PATENT APPLICATION**

(43) Date of publication:
25.03.1998 Bulletin 1998/13

(51) Int. Cl.^{6}: H04L 27/233

(21) Application number: 97120803.8

(22) Date of filing: 24.12.1992

(84) Designated Contracting States:
DE FR GB IT SE

(30) Priority: 27.12.1991 JP 347245/91
12.03.1992 JP 53583/92
25.03.1992 JP 67124/92

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
92121972.1 / 0 548 982

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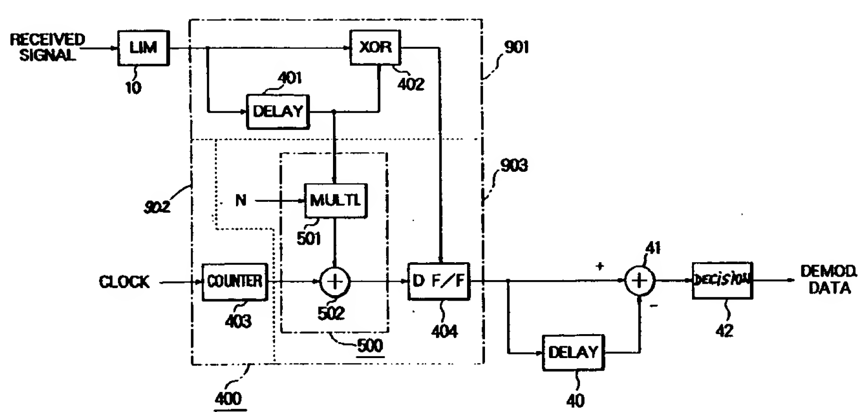
Remarks:
This application was filed on 27 - 11 - 1997 as a divisional application to the application mentioned under INID code 62.

(54) **Phase detection circuit and differential detection demodulator**

(57) A phase detection circuit (400) for detecting a phase shift of an input signal relative to a phase referenced signal and for generating a relative phase signal includes: a half-period detection means (901) consisting of a delay element (401) and an exclusives OR element (402); a phase reference signal generation means (902) consisting of a modulo 2N counter (403); and a phase shift measurement means (903) consisting of a phase inversion corrector (500) and a D flip-flop array (404). A delay element (40) delays the relative phase signal by one symbol period and a subtractor (41) outputs the phase difference signal representing the phase transition over each symbol period of the received signal. A decision circuit (42) obtains the demodulated data from the phase difference signal.

FIG. 1



EP 0 831 625 A2

Printed by Xerox (UK) Business Services
2.15.12/3.4

Description

The present invention relates to a detection circuit for detecting a phase shift of an input signal relative to a phase reference signal and to a differential detection demodulator.

In the following, a differential detection demodulator using a phase detection circuit ist described. A digital differential detection demodulator using a phase detection circuit is disclosed, for example, in H. Tomita et al., "DIGITAL INTERMEDIATE FREQUENCY DEMODULATION TECHNIQUE", Paper B-299, 1990 Fall National Conference of the Institute of Electronics, Information and Communication Engineers of Japan. The differential detection demodulator is described by reference to drawings.

Fig. 11 is a block diagram showing the structure of a digital differential detection demodulator provided with a phase detection circuit. First, the received signal is supplied to a limiter amplifier 10. The output of the limiter amplifier 10 is coupled to a phase detection circuit 200 including: a counter 201 counting in modulo K, where K is a positive integer; and a D flip-flop array 202. The output of the phase detection circuit 200 is coupled to: a delay element 40 having a delay time equal to the one symbol period of the received signal; and a subtractor 41 effecting subtraction in modulo 2π.

Next the operation of the circuit of Fig. 11 is described. The received signal, which is a differential phase shift keying (DPSK) signal, is shaped by the limiter amplifier 10 into a rectangular waveform of constant amplitude. Namely, the limiter amplifier 10 acts as a quantizer for effecting 2-level quantization upon the received signal. Thus, the received signal is quantized by the limiter amplifier 10 into a 2-level signal taking the value either at the logical "0" or logical "1".

The counter 201 of modulo K within the phase detection circuit 200 is supplied a clock signal having a frequency pratically equal to K times the frequency of the received signal. The output of the counter 201 is supplied to the D flip-flop array 202, which is driven by the 2-level quantized received signal output from the limiter amplifier 10. The output of the phase detection circuit 200 represents the relative phase of the 2-level quantized received signal with respect to a virtual phase reference signal.

Next this is described by reference to waveform diagrams. Figs. 12 and 13 are timing charts showing the waveforms exemplifying the operation of the phase detection circuit 200, where K=16. In Fig. 12 are shown, from top to bottom, the waveforms of: the clock supplied to the counter 201; the output of the counter 201; the virtual phase reference signal, which is obtained by demultiplying the clock of the counter 201 by K (equal to 16 in this case); the 2-level quantized received signal; and the output of the D flip-flop array 202. From top to bottom in Fig. 13 are shown the waveforms of: the clock for the counter 201; the output of the counter 201; the virtual phase reference signal; the 2-level quantized received signal A, the phase of which is increasingly lagged; output A of D flip-flop array 202 corresponding to the 2-level quantized received signal A; the 2-level quantized received signal B, the phase of which is increasingly led; and the output B of the D flip-flop array 202 corresponding to the 2-level quantized received signal B.

The virtual phase reference signal rises to logical "1" at the instant when the output of the counter 201 is reset to logical "0", and falls to logical "0" at the instant when the output of the counter 201 reaches K/2 (equal to 8 in this case). If the period of the clock of the counter 201 is represented by T and that of the virtual phase reference signal T_r, then:

$$t_r = K T$$

Thus, if the length of time between the rising edges of the virtual phase reference signal and the 2-level quantized received signal is represented by τ, then the phase shift φ of the 2-level quantized received signal relative to the virtual phase reference signal is given by:

$$\varphi = 2 \pi \tau / T_r = 2 \pi \tau / (K T).$$

On the other hand, as seen from Fig. 12, the output of the counter 201 at the rising edge of the 2-level quantized received signal is equal to an integer obtained by dividing the time τ by the period T of the clock of the counter 201 and then discarding the fractional parts of the quotient.

The D flip-flop array 202 is driven at each rising edge of the 2-level quantized received signal to hold the output of the counter 201. Thus, the output of the D flip-flop array 202 is equal to the integer obtained by dividing the shift time τ by the period T of the clock of the counter 201 and then discarding the fractional parts of the quotient resulting from the division. Namely, if the output of the D flip-flop array 202 is represented by μ, where $\mu \varepsilon \{0, 1, ..., K-1\}$, then the following relation holds among μ, T and τ:

$$\mu \leq \tau / T < (\mu + 1).$$

Thus, the following relation holds between the phase shift φ of the 2-level quantized received signal relative to the virtual phase reference signal and the output μ of the D flip-flop array 202:

$$2 \pi \mu / K \leq \varphi < 2 \pi (\mu + 1) / K.$$

This relation shows that the output of the D flip-flop array 202 cn be regarded as the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal.

Fig. 12 shows the case where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal is constant. Thus, the out-

put of the D flip-flop array 202 remains at eight (8). On the other hand, Fig. 13 shows the case where the relative phase signal of the 2-level quantized received signal A is increasingly lagging and the relative phase signal of the 2-level quantized received signal B is increasingly leading. Thus, upon receiving the 2-level quantized received signal A, the output A of the D flip-flop array 202 increases from seven (7) to nine (9). On the other hand, upon receiving the 2-level quantized received signal B, the output B of the D flip-flop array 202 decreases from nine (9) to seven (7). In either case, the output of the D flip-flop array 202 varies in proportion to the variation of the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal.

The output of the phase detection circuit 200 supplied to the subtractor 41 and the delay element 40. At the delay element 40 the relative phase signal is delayed by one symbol period of the received signal and then is supplied to the subtractor 41. The subtractor 41 subtracts, in modulo 2π, the output of the D flip-flop array 202 from the output of the phase detection circuit 200, and thereby obtains the phase difference signal. The decision circuit 42 obtains the demodulated data on the basis of the predetermined correspondence relationship between the phase difference signal and the demodulated data.

The phase detection circuit of Fig. 11 has the following disadvantage. The D flip-flop array 202 is driven only at the rising edges of the 2-level quantized received signal. Thus, the relative phase signal output from the phase detection circuit is updated only at each full period of the 2-level quantized received signal. In principle, however, the value of the relative phase of the 2-level quantized received signal can be updated two times for each period of the 2-level quantized received signal. Namely, the phase detection circuit of Fig. 11 has the disadvantage that the rate at which the relative phase signal is updated is low.

It is, therefore, the object of the present invention to shorten the update period of the known phase detection circuit.

This object according to the present invention is solved by the features of claims 1 and 7, respectively. Preferred embodiments of the phase detection circuit and the differential detection demodulator, respectively, in compliance with this invention are defined in the respective subclaims.

The phase detection circuit according to this invention for detecting a phase shift of an input signal relative to a phase reference signal, comprises: half-period detection means for generating, in response to the input signal, a half-period detection signal at each half-period of the input signal; phase reference signal generation means for generating the phase reference signal in response to a clock signal having a frequency not less than twice a frequency of the input signal; and phase shift measurement means, coupled to the half-period detection means and phase reference signal generation means and including phase inversion correction means for correcting the phase reference siganl for a phase inversion thereof at each alternate half-period of the input signal, the phase shift measurement means measuring and outputting a phase shift of the input signal with respect to the phase reference signal at each half-period of the input signal, on the basis of the phase reference signal corrected by the phase inversion correction means and the half-period detection signal output from the half-period detection means.

Preferably, the half-period detection means includes: a delay element for delaying the input signal by a delay time shorter than the half-period of the input signal; and a first exclusive OR element for generating a logical exclusive OR of the input signal and an output of the delay element; the phase reference signal generation means includes a counter for counting in modulo 2N a clock signal having a frequency practically equal to 2N times the frequency of the input signal, where N is a positive integer; the phase inversion correction means adds a numerical value "0" or "N" in modulo 2N to an output of the counter in response to the output of the delay element in the half-period detected; and the phase shift measurement means includes, in addition to the phase inversion correction means, a D flip-flop array coupled to the phase inversion correction means and the first exclusive OR element, the D flip-flop array holding an output of the phase inversion correction means in response to the logical exclusive OR output of the exclusive OR element, wherein a value held in the D flip-flop array constitutes an output of the phase shift measurement means.

Further, the phase inversion correction means may include: a multiplier coupled to the delay element, for multiplying the output of the delay element by N; and an adder coupled to the counter and the multiplier, for adding an output of the multiplier to the output of the counter in modulo 2N.

Alternatively, the phase inversion correction means may include: a data selector coupled to the delay element, for selecting a numerical value "0" when the output of the delay element is a logical "0", and a numerical value "1" when the output of the delay element is at logical "1"; and an adder coupled to the counter and the data selector, for adding an output of the data selector to the output of the counter in modulo 2N.

Still alternatively, the phase inversion correction means may include: logical product elements coupled to the delay element, for generating logical products of the output of the delay element and respective bits of a numerical value "N"; and an adder coupled to the counter and the logical product elements, for adding outputs of the logical product elements with the output of the counter in modulo 2N.

Preferably, the counter counts a clock signal having a frequency practically equalto 2^M times the frequency of the input signal, where M is a positive integer; and the

phase inversion corrector means includes a second exclusive OR element coupled to the output of the delay element and a most significant bit of the output of the counter, the second exclusive OR element generating a logical exclusive OR of the output of the delay element and the most significant bit of the output of the counter, wherein an output of the phase inversion corrector means consists of a combination of least significant bits of the output of the modulo 2N counter and the logical exclusive OR output of the second exclusive OR element.

According to an alternative aspect of this invention, the differential detection demodulator for demodulating a 2-level quantized received signal using a phase reference signal having a fixed frequency practically equal to a frequency of the received signal, the differential detection demodulator comprises: half-period detection means for generating, in response to the received signal, a half-period detection signal at each half-period of the received signal; phase reference signal generation means for generating the phase reference signal in response to a clock signal having a frequency not less than twice the frequency of the received signal; phase shift measurement means, coupled to the half-period detection means and phase reference signal generation means and including phase inversion correction means for correcting the phase reference signal for a phase inversion thereof at each alternate half-period of the received signal, the phase shift measurement means outputting a relative phase signal representing a relative phase of the received signal with respect to the phase reference signal at each half-period of the received signal, on the basis of the phase reference signal corrected by the phase inversion correction means and the half-period detection signal output from the half-period detection means; a delay element coupled to the phase shift determiner means, for delaying the relative phase signal output from the phase shift measurement means by one symbol period of the received signal; and a subtractor coupled to the phase shift measurement means and the delay element, for subtacting an output of the delay element from the relative phase signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The features which are believed to be characteristic of this invention are set forth with particularity in the appended claims. The structure and method of operation of this invention itself, however, will be best understood from the following detailed description, taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram of a differential detection demodulator provided with a phase detection circuit according to this invention, by which the value of the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal can be updated two times for each period of the 2-level quantized received signal;

Fig. 2 is a timing chart showing waveforms exemplifying the operation of the delay element 401 and the exclusive OR element 402 of Fig. 2;

Fig. 3 ist a timing chart exemplifying the waveforms of the output of the modulo 2N counter 403, the virtual phase reference signal, the 2-level quantized received signal, and the differential pulse signal of Fig. 1, in the case where N = 8;

Fig. 4 is a timing chart showing the wave-forms exemplifying the operation of the phase detection circuit 400 of Fig. 1, where N = 8 (2N = 16) and where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal remains constant;

Fig. 5 is a view similar to that of Fig. 4, but showing the case where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal lags increasingly;

Fig. 6 is a view similar to that of Fig. 4, but showing the case where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal leads increasingly;

Fig. 7 is a block diagram of another differential detection demodulator provided with a phase detection circuit according to this invention, by which the value of the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal can be updated two times for each period of the 2-level quantized received signal;

Fig. 8 is a timing chart showing the waveforms exemplifying the operation of the phase detection circuit 400a of Fig. 7, where M = 4 ($2^M = 16$) and where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal remains constant;

Fig. 9 is a view similar to that of Fig. 8, but showing the case where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal lags increasingly;

Fig. 10 is a view similar to that of Fig. 8, but showing the case where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal leads increasingly;

Fig. 11 is a block diagram showing the structure of a conventional digital differential detection demodulator provided with a phase detection circuit;

Fig. 12 is a timing chart showing waveforms exemplifying the operation of phase detection circuit of Fig. 11 in the case where the relative phase of the received signal with respect to the virtual phase reference signal remains constant; and

Fig. 13 is a timing chart showing waveforms exemplifying the operation of a phase detection circuit of Fig. 11, in the case where the relative phase of the received signal with respect to the virtual phase reference signal varies.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the accompanying drawings, the preferred embodiments of this invention are described.

Fig. 1 is a block diagram of a differential detection demodulator provided with a phase detection circuit according to this invention, by which the value of the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal can be updated two times for each period of the 2-level quantized received signal. The output of limiter amplifier 10 is coupled to a phase detection circuit 400 which includes: a delay element 401 and an exclusive OR element 402 coupled to the limiter amplifier 10; a modulo 2N counter 403 for counting in modulo 2N, where N is a positive integer; a D flip-flop array 404; and a phase inversion corrector 500. The phase inversion corrector 500 includes: a multiplier 501 and an adder 502 for effecting addition in modulo 2N.

Functionally, the phase detection circuit 400 is divided into a half-period detection means 901, a phase reference signal generation means 902 and a phase shift measurement means 903. The half-period detection means 901 consists of the delay element 401 and the exclusive OR element 402. Upon receiving the 2-level quantized received signal from the limiter amplifier 10, the half-period detector means 901 outputs a half-period detection signal at each half-period of the received signal. The phase reference signal generation means 902 consists of the modulo 2N counter 403. On the basis of a clock signal having a frequency not less than twice the frequency of the input signal, the phase reference signal generation means 902 generates the phase reference signal serving as the reference for measuring the phase shift of the 2-level quantized received signal. A phase shift measurement means 903 consists of the D flip-flop array 404 and the phase inversion corrector 500. The phase inversion corrector 500 corrects the phase inversion of the phase reference signal at each half-period of the received signal. On the basis of the corrected phase reference signal and the half-period detection signal output from the half-period detection means 901, the phase shift measurement means 903 determines and outputs the phase shift of the 2-level quantized received signal relative to the phase reference signal at each half-period of the received signal.

The delay element 40, subtractor 41, and the decision circuit 42 are similar to those described above.

Next, the operation of the circuit of Fig. 1 is described in detail. In Fig. 1, the limiter amplifier 10 shapes the received signal into a rectangular wave-form of a constant amplitude. Namely, the limiter amplifier 10 acts as a 2-level quantizer for subjecting the received signal to the 2-level quantization, such that the output of the limiter amplifier 10 is quantized to logical "0" and "1".

The 2-level quantized received signal output from the limiter amplifier 10 is supplied to the phase detection circuit 400, where it is first input to the delay element 401. The delay time of the delay element 401 is shorter than the half-period of the 2-level quantized received signal. The delayed received signal output from the delay element 401 is supplied to the exclusive OR element 402, together with the 2-level quantized received signal output from the limiter amplifier 10. The exclusive OR element 402 effects the logical exclusive OR operation upon the outputs of the limiter amplifier 10 and the delay element 401. Thus, the output of the exclusive OR element 402 is a pulse signal (referred to as the differential pulse signal) which rises (i.e., has rising edges) at the rising and the falling edges of the 2-level quantized received signal. Next, this is described by reference to drawings.

Fig. 2 is a timing chart showing waveforms exemplifying the operation of the delay element 401 and the exclusive OR element 402 of Fig. 1. From top to bottom in Fig. 2 are shown the waveforms of: the 2-level quantized received signal; the output of the delay element 401; and the output of the exclusive OR element 402 (the differential pulse signal). As shown in Fig. 2, the delay time of the delay element 401, namely the time length by which the 2-level quantized received signal is delayed, is shorter than the half-period of the 2-level quantized received signal. Thus, the differential pulse signal output from the exclusive OR element 402 rises (i.e., has the rising edges) at the rising and the falling edges of the 2-level quantized received signal.

On the other hand, the modulo 2N counter 403 is driven by a clock signal having a frequency practically equal to 2N times the frequency of the 2-level quantized

received signal. If a virtual phase reference signal similar to that of Fig. 11 is assumed which is obtained by demultiplying the clock signal of the modulo 2N counter 403 by 2N, the virtual phase reference signal rises (i.e., has the rising edge) at the instant when the output of the modulo 2N counter 403 is reset to "0", and falls (i.e., has the falling edge) at the instant when the output of the modulo 2N counter 403 reaches N. The output of the modulo 2N counter 403 represents the phase of this virtual phase reference signal. Namely, if the output of the modulo 2N counter 403 at the time when the phase of the virtual phase reference signal is θ is represented by α ($\alpha \varepsilon \{0, 1, ..., 2N-1\}$), then the following relation holds between θ and α:

$$\pi\alpha / N \leq \theta < \pi(\alpha + 1) / N$$

Thus, the output of the modulo 2N counter 403 at each rising edge of the differential pulse signal output from the exclusive OR element 402 represents the phase of the virtual phase reference signal at the rising or the falling edge of the 2-level quantized received signal. However, the absolute phase of the 2-level quantized received signal at the falling edge is equal to π. Thus, if the output of the modulo 2N counter 403 at the falling edge of the 2-level quantized received signal is corrected by numerical value "N" corresponding to the phase π, then the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal at the falling edge of the 2-level quantized received signal can be obtained. Next, this is described by reference to drawings.

Fig. 3 is a timing chart exemplifying the waveforms of the output of the modulo 2N counter 403, the virtual phase reference signal, the 2-level quantized received signal, and the differential pulse signal of Fig. 1, in the case where N = 8. From top to bottom are shown the waveforms of: the clock signal for the modulo 2N counter 403; the output of the modulo 2N counter 403; the virtual phase reference signal; the 2-level quantized received signal; the delayed received signal (output of the delay element 401); and the differential pulse signal (output of the exclusive OR element 402). The modulo 2N counter 403 counts the clock signal in modulo 2N = 16.

Let the periods of the clock signal of the modulo 2N counter 403 and the virtual phase reference signal be represented by T and T_r, respectively. Then:

$$T_r = 2N \cdot T.$$

Thus, if the time length between the rising or the falling edges of the virtual phase reference signal and the 2-level quantized received signal is represented by τ, the phase shift φ of the 2-level quantized received signal relative to the virtual phase reference signal is given by:

$$\varphi = 2\pi \cdot \tau / T_r = \pi\tau / (N \cdot T).$$

Further, let the output of the modulo 2N counter 403 at a rising edge of the 2-level quantized received signal be represented by β_1, where $\beta_1 \varepsilon \{0, 1, ..., 2N-1\}$. Then β_1 is equal to an integer obtained by first normalizing (i.e., dividing) the time τ, between the rising edges of the virtual phase reference signal and teh 2-level quantized received signal, by the period T of the modulo 2N counter 403 and then discarding the fractional part of the quotient resulting from the division. Namely, the following relation holds among β_1, T and τ:

$$\beta_1 \leq \tau / T < (\beta_1 + 1).$$

On the other hand, the output of the modulo 2N counter 403 at the falling edge of the virtual phase reference signal is equal to "N" (= 8 in the case of Fig. 3) corresponding to the phase π. Let the output of the modulo 2N counter 403 at a falling edge of the 2-level quantized received signal be represented by β_2, where $\beta_2 \varepsilon \{0, 1, ..., 2N-1\}$. Then β_2 is equal to an integer obtained by: first normalizing (i.e., dividing) the time τ between teh falling edges of the virtual phase reference signal and the 2-level quantized received signal by the period T of the modulo 2N counter 403; then discarding the fractional part of the quotient resulting from the division; and finally subtracting numerical value "N" to the quotient. Thus, the following relation holds among β_2, T and τ:

$$(\beta_2 - N) \leq \tau / T < (\beta_2 - N + 1).$$

The subtraction in the above equation is in modulo 2N. Subtracting "N" in modulo 2N, however, is equivalent to adding "N" in modulo 2N. Thus the above equation is equivalent to:

$$(\beta_2 + N) \leq \tau / T < (\beta_2 + N + 1).$$

From the above discussion, it has been shown that the following relations hold among the output of the modulo 2N counter 403, β_1 and β_2, and the phase shift φ of the 2-level quantized received signal:

$$\pi\beta_1 / N \leq \varphi < \pi(\beta_1 + 1)/N$$

$$\pi(\beta_2 + N) \leq \varphi < (\beta_2 + N + 1)/N.$$

These relations show that the output β_1 of the modulo 2N counter 403 at the rising edge of the 2-level quantized received signal and the value obtained by adding numerical value "N" in modulo 2N to th output β_2 of the modulo 2N counter 403 at the falling edge of the 2-level quantized received signal can be regarded as representing the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal. In other words, the relative phase of teh 2-level quantized received signal can be obtained by cor-

recting theh output of the modulo 2N counter 403, i.e., by adding the numerical value "0" at the rising edge, and the numerical value "N" at the falling edge, of the 2-level quantized received signal.

The phase inversion corrector 500 effects this correction for the output of the modulo 2N counter 403. Namely, upon receiving the output of the modulo 2N counter 403, the phase inversion corrector 500 adds to it the numerical value "0" at the rising edge, and the numerical value "N" at the falling edge, of the 2-level quantized received signal. Next, the operation of the phase inversion corrector 500 is described by reference to drawings.

Fig. 4 is a timing chart showing the waveforms exemplifying the operation of the phase detection circuit 400 of Fig. 1, where N = 8 (2N = 16) and where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal remains constant. Fig. 5 is a view similar to that of Fig.4, but showing the case where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal lags increasingly. Fig. 6 is a view similar to that of Fig. 4, but showing the case where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal leads increasingly. From top to bottom in the figures are shown the waveforms of: the clock signal for the modulo 2N counter 403; the output of the modulo 2N counter 403; the virtual phase reference signal; the 2-level quantized received signal; the delayed received signal (output of the delay element 401); the differential pulse signal (output of the exclusive OR element 402); the output of the multiplier 501; the output of the adder 502; and the output of the D flip-flop array 404.

As shown in these figures, the value of the delayed received signal output from the delay element 401 is at logical "0" at the rising edge, and at logical "1" at the falling edge, of the 2-level quantized received signal. The multiplier 501 multiplies output of the delay element 401 by N, thereby outputting the numerical value "0" at the rising edge, and the numerical value "N" at the falling edge, of the 2-level quantized received signal. The adder 502 adds in modulo 2N the outputs of the modulo 2N counter 403 and the multiplier 501, thereby obtaining the output of the phase inversion corrector 500. The output of the phase inversion corrector 500 is equal to the output of the modulo 2N counter 403 at the rising edge of teh 2-level quantized received signal. The output of the phase inversion corrector 500 is equal to the value obtained by adding in modulo 2N the numerical value "N" to the output of the modulo 2N counter 403, at the falling edge of the 2-level quantized received signal.

The output of the phase inversion corrector 500 is supplied to the D flip-flop array 404, which is driven by the differential pulse signal output from the exclusive OR element 402. As described above, the differential pulse signal has rising edges at the rising and falling edges of the 2-level quantized received signal. Thus, the D flip-flop array 404 is driven at each rising and falling edge of the 2-level quantized received signal. Thus, if the output of the D flip-flop array 404 is represented by μ, then μ is expressed in terms of the output values β_1 and β_2 of the modulo 2N counter 403 at the rising and the falling edges, respectively:

$$\mu = \beta_1$$

$$\mu = \beta_2 + N$$

Thus, the following relation holds between the phase shift φ of the 2-level quantized received signal with respect to the virtual phase reference signal and the output μ of the D flip-flop array 404:

$$\pi \mu / N \leq \varphi < \pi (\mu + 1)/N$$

This relation shows that the output μ of the D flip-flop array 404 can be regarded as representing the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal. This can be easily understood by reference to Figs. 4 through 6.

It is noted that in the case of the circuit of Fig. 11, the output of the D flip-flop array 202 representing the relative phase of the 2-level quantized received signal is updated only once for each period of the 2-level quantized received signal. In the case of the circuit of Fig. 1, however, the D flip-flop array 404 is driven by the differential pulse signal at the rising and the falling edges of the 2-level quantized received signal. Thus, the output of the D flip-flop array 404 representing the relative phase of the 2-level quantized received signal is updated twice for each period of the 2-level quantized received signal. The updating rate of the relative phase signal is thereby doubled. This can be easily comprehended by comparing Fig. 4 with Fig. 12 and Figs. 5 and 6 with Fig. 13.

Namely, the 2-level quantized received signal A of Fig. 13 and the 2-level quantized received signal of Fig. 5 are the same.The output A of the D flip-flop array 202 in Fig. 13 varies from "7" to "9", while the output of the D flip-flop array 404 in Fig. 5 varies gradually from "7" to "8" to "9". Similarly, the 2-level quantized received signal B of Fig. 13 and teh 2-level quantized received signal of Fig. 6 are the same. The output B of the D flip-flop array 202 in Fig. 13 varies from "9" to "7", while the output of the D flip-flop array 404 in Fig. 6 varies gradually from "9" to "8" to "7". The updating rate of the relative phase signal is doubled for the circuit of Fig. 1, and hence the variation of the value of the relative phase signal is rendered less abrupt.

The operations of the delay element 40, the subtractor 41, and the decision circuit 42 are similar to those of the corresponding parts described above.

In Fig. 1, the phase inversion corrector 500 consists of the multiplier 501 and the adder 502. However, the element corresponding to the multiplier 501 may be

implemented by any circuit which outputs numerical value "0" upon receiving numerical value "0", and numerical value "N" upon receiving numerical value "1". Such element may be implemented by a data selector which selects and outputs numerical value "0" upon receiving numerical value "0", and numerical value "N" upon receiving numerical value "1". Alternatively, the phase inversion corrector 500 may consist of logical product elements (AND gates) for effecting logical product operations (AND operations) upon the respective bits of the numerical value "N" and the output of the delay element 401.

The above description relates to the case where the received signal is modulated in accordance with the differential phase shift keying (DPSK). This invention, however, can also be applied to MSK or GMSK modulation systems. Further, in the case of the above embodiment, the constant N serving as the operation parameter of the phase detection circuit 400 is equal to 8 (N = 8). However, the constant N may be any positive integer. For example, N may be N = 16 or N = 32.

Fig. 7 is a block diagram of another differential detection demodulator provided with a phase detection circuit according to this invention, by which the value of the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal can be updated two times for each period of the 2-level quantized received signal. In Fig. 7, the phase detection circuit 400a is functionally divided into: a half-period detection means 901 consisting of the delay element 401 and the exclusive OR element 402; a phase reference signal generation means 902 consisting of the modulo 2^M counter 403a, where M is a positive integer; and a phase shift measurement means 903 consisting of the D flip-flop array 404a and a phase inversion corrector 500a. The phase inversion corrector 500a consists of an exclusive OR element 503 having inputs coupled to the output of the delay element 401 and the most significant bit (MSB) of the output of the modulo 2^M counter 403a. The combination of the least significant bits (namely the first through (M - 1)th bit of the modulo 2^M counter 403a) and the output of the exclusive OR element 503 is input to the D flip-flop array 404a.

Otherwise the circuit of Fig. 7 is similar to the circuit of Fig. 1.

Next, the operation of the circuit of Fig. 7 is described in detail. In Fig. 7, the limiter amplifier 10 shapes the received signal into a rectangular waveform of a constant amplitude. Namely, the limiter amplifier 10 acts as a 2-level quantizer for subjecting the received signal to the 2-level quantization, such that the output of the limiter amplifier 10 is quantized to logical "0" and "1".

The 2-level quantized received signal output from the limiter amplifier 10 is supplied to the phase detection circuit 400a, where it is first input to the delay element 401 and the exclusive OR element 402. The delay time of the delay element 401 is shorter than the half-period of the 2-level quantized received signal. The delayed received signal output from the delay element 401 is supplied to the exclusive OR element 402. The exclusive OR element 402 effects the logical exclusive OR operation upon the outputs of the limiter amplifier 10 and the delay element 401. Thus, the output of the exclusive OR element 402 is a pulse signal (referred to as the differential pulse signal) which rises (i.e., has rising edges) at the rising and the falling edges of the 2-level quantized received signal.

The modulo 2^M counter 403a is driven by a clock signal having a frequency practically equal to 2^M times the frequency of the 2-level quantized received signal, where M is a positive integer. If a virtual phase reference signal similar to that of Fig. 9 is assumed which is obtained by demultiplying the clock signal of the modulo 2^M counter 403a by 2^M, the virtual phase reference signal rises (i.e., has the rising edge) at the instant when the output of the modulo 2^M counter 403a is reset to "0", and falls (i.e., has the falling edge) at the instant when the output of the modulo 2^M counter 403a reaches 2^{M-1}. The output of the modulo 2^M counter 403a represents the phase of this virtual phase reference signal. Namely, if the output of the modulo 2^M counter 403a at the time when the phase of the virtual phase reference signal is θ is represented by α ($\alpha \in \{0, 1, ..., 2^M - 1\}$), then the following relation holds between θ and α:

$$2\pi\alpha/2^M \leq \theta < 2\pi(\alpha + 1)/2^M.$$

Thus, the output of the modulo 2^M counter 403a at each rising edge of the differential pulse signal output from the exclusive OR element 402 represents the phase of the virtual phase reference signal at the rising or the falling edge of the 2-level quantized received signal. However, the absolute phase of the 2-level quantized received signal at the falling edge is equal to π. Thus, if the output of the modulo 2^M counter 403a at the falling edge of the 2-level quantized received signal is corrected by numerical value "2^{M-1}" corresponding to the phase π, then the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal at the falling edge of the 2-level quantized received signal can be obtained.

The phase inversion corrector 500a effects this correction for the output of the modulo 2^M counter 403a. Namely, upon receiving the output of the modulo 2^M counter 403a, the phase inversion corrector 500a adds to it the numerical value "0" at the rising edge, and the numerical value "2^{M-1}" at the falling edge, of the 2-level quantized received signal. Next, the operation of the phase inversion corrector 500a is described by reference to drawings.

Fig. 8 is a timing chart showing the waveforms exemplifying the operation of the phase detection circuit 400a of Fig. 7, where M = 4 (2^M = 16) and where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal remains

constant. Fig. 9 is a view similar to that of Fig. 8, but showing the case where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal lags increasingly. Fig. 10 is a view similar to that of Fig. 8, but showing the case where the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal is increasingly led. From top to bottom in the respective figures are shown the waveforms of: the clock signal for the modulo 2^M counter 403a; the output of the modulo 2^M counter 403a; the MSB or the most significant bit (the Mth bit) of the modulo 2^M counter 403a; the 2-level quantized received signal; the delayed received signal (output of the delay element 401); the differential pulse signal (output of the exclusive OR element 402); the output of the exclusive OR element 503; the LSBs or the least significant bits (the first through (M - 1)th bits) of the modulo 2^M counter 403a; the output of the phase inversion corrector 500a (the combination of the least significant bits of the modulo 2^M counter 403a and the output of the exclusive OR element 503; and the output of the D flip-flop array 404a. The numbers at the waveforms of the modulo 2^M counter 403a, the least significant bits of the 403a, the phase inversion corrector 500a, and the D flip-flop array 404a represent the values thereof at respective instants.

The output of the modulo 2^M counter 403a consists of M bits. The most significant bit of the modulo 2^M counter 403a represents the numerical value 2^{M-1}. Thus, adding the numerical value 2^{M-1} to the output of teh modulo 2^M counter 403a in modulo 2^M is equivalent to logical inversion of the most significant bit of the modulo 2^M counter 403a. Thus, adding numerical value "0" and "2^{M-1}", respectively, to the output of the modulo 2^M counter 403a at the rising and the falling edges of the 2-level quantized received signal results in effecting no logical inversion at the rising edge, and the logical inversion at the falling edge, of the 2-level quantized received signal, upon the most significant bit of the modulo 2^M counter 403a.

As shown in Figs. 8 through 10, the value of the delayed received signal output from the delay element 401 is at logical "0" at the rising edge, and at logical "1" at the falling edge, of the 2-level quantized received signal. The exclusive OR element 503 effects the logical exclusive OR operation upon the delayed received siganl output from the delay element 401 and the most significant bit of the output from the modulo 2^M counter 403a. The output of the 503 is combined as the new most significant bit with the least significant bits (the first through (M-1)th bits) of the modulo 2^M counter 403a, to form the output of the phase inversion corrector 500a. Thus, the output of the phase inversion corrector 500a is equal to the output of the modulo 2^M counter 403a at the rising edges of the 2-level quantized received signal (no logical inversion of the most significant bit is effected). On the other hand, the outpur of the phase inversion corrector 500a at the falling edges of the 2-level quantized received signal consists of the logically inverted most significant bit of the modulo 2^M counter 403a combined with the least significant bits thereof. Thus, the output of the phase inversion corrector 500a is equal to the value obtained by adding numerical value "0" at the rising edge, and numerical value "2^{M-1}" at the falling edge, of the 2-level quantized received signal, to the output of the modulo 2^M counter 403a.

By limiting the constant 2N serving as the operation parameter in the circuit of Fig. 1 to the integer which can be expressed in the form 2^M, the phase inversion corrector 500a can be implemented only by the exclusive OR element 503. Thus, the circuit of Fig. 7 is simplified compared to the circuit of Fig. 1.

The output of the phase inversion corrector 500a is supplied to the D flip-flop array 404a, which is driven by the differential pulse signal output from the exclusive OR element 402. As described above, the differential pulse signal has rising edges at the rising and falling edges of the 2-level quantized received signal. Thus, the D flip-flop array 404a is driven at each rising and falling edge of the 2-level quantized received signal. Thus, if the output of the D flip-flop array 404a is represented by μ, where $\mu \in \{0, 1, ..., 2^M-1\}$, then μ is expressed in terms of the output values β_1 and β_2 ($\beta_1, \beta_2 \in \{0, 1, ..., 2^M - 1\}$) of the modulo 2^M counter 403a at the rising and the falling edges, respectively:

$$\mu = \beta_1$$

$$\mu = \beta_2 + 2^{M-1}$$

Thus, the following relation holds between the phase shift φ of the 2-level quantized received signal with respect to the virtual phase reference signal and the output μ of the D flip-flop array 404a:

$$2\pi\mu/2^M \leq \varphi < 2\pi(\mu+1)/2^M$$

This relation shows that the output μ of the D flip-flop array 404a can be regarded as representing the relative phase of the 2-level quantized received signal with respect to the virtual phase reference signal. This can be easily understood by reference to Figs. 8 through 10.

As in the case of the circuit of Fig. 1, the D flip-flop array 404a of Fig. 7 is driven by the differential pulse signal at the rising and the falling edges of the 2-level quantized received signal. Thus, the output of the D flip-flop array 404a representing the relative phase of the 2-level quantized received signal is updated twice for each period of the 2-level quantized received signal. The updating rate of the relative phase signal is thereby doubled compared to the case of Fig. 11. This can be easily comprehended by comparing Fig. 8 with Fig. 12 and Figs. 9 and 10 with Fig. 13.

Namely, the 2-level quantized received signal A of Fig. 13 and the 2-level quantized received signal of Fig. 9 are the same. The output A of the D flip-flop array 202

in Fig. 13 varies from "7" to "9", while the output of the D flip-flop array 404a in Fig. 9 varies gradually from "7" to "8" to "9". Similarly, the 2-level quantized received signal B of Fig. 13 and the 2-level quantized received signal of Fig. 10 are the same. The output B of the D flip-flop array 202 in Fig. 13 varies from "9" to "7", while the output of the D flip-flop array 404a in Fig. 10 varies gradually from "9" to "8" to "7". The updating rate of the relative phase signal is doubled for the circuit of Fig. 7, and hence the variation of the value of the relative phase signal is rendered less abrupt.

The operations of the delay element 40, the subtractor 41, and teh decision circuit 42 of Fig. 7 are the same as those of the corresponding parts described above.

The above description relates to the case where the received signal is modulated in accordance with the differential phase shift keying (DPSK). However, the principle embodied in the circuit of Fig. 7 can be applied to MSK or GMSK modulation systems. Further, in the case of the above embodiment, the constant M serving as the operation parameter of the phase detection circuit 400a is equal to 4 (M=4). However, the constant M may be any positive integer. For example, M may be five (M=5) or six (M=6).

Claims

1. A phase detection circuit for detecting a phase shift of an input signal relative to a phase reference signal, comprising:

    half-period detection means (901) for generating, in response to said input signal, a half-period detection signal at each half-period of said input signal;
    phase reference signal generation means (902) for generating said phase reference signal in response to a clock having a frequency not less than twice a frequency of said input signal;
    and
    phase shift measurement means (903), coupled to said half-period detection means (901) and phase reference signal generation means (902) and including phase inversion correction means (500) for correcting said phase reference signal for a phase inversion thereof at each alternate half-period of said input signal, said phase shift measurement means (903) measuring and outputting a phase shift of said input signal with respect to said phase reference signal at each half-period of said input signal, on the basis of said phase reference signal corrected by said phase inversion correction means (500) and said half-period detection signal output from said half-period detection means (901).

2. A phase detection circuit as claimed in claim 1, wherein:

    said half-period detection means (901) includes: a delay element (401) for delaying said input signal by a delay time shorter than said half-period of said input signal; and a first exclusive OR element (402) for generating a logical exclusive OR of said input signal and an output of said delay element (401);
    said phase reference signal generation means (902) includes a counter (403) for counting in modulo 2N a clock having a frequency practically equal to 2N times said frequency of said input signal, where N is a positive integer;
    said phase inversion correction means (500) adds a numerical value "0" or "N" in modulo 2N to an output of said counter (403) in response to said output of said delay element (401); and
    said phase shift measurement means (903) includes, in addition to said phase inversion correction means (500), a D flip-flop array (404) coupled to said phase inversion correction means (500) and said first exclusive OR element (402), said D flip-flop array (404) holding an output of said phase inversion correction means (500) in response to said logical exclusive OR output of said exclusive OR element (402), wherein a value held in said D flip-flop array (404) constitutes an output of said phase shift measurement means (903).

3. A phase detection circuit as claimed in claim 2, wherein said phase inversion correction means (500) includes:

    a multiplier (501) coupled to said delay element (401), for multiplying said output of said delay element (401) by N; and
    an adder (502) coupled to said counter (403) and said multiplier (501), for adding an output of said multiplier (501) to said output of said counter (403) in modulo 2N.

4. A phase detection circuit as claimed in claim 2, wherein said phase inversion correction means includes:

    a data selector coupled to said delay element, for selecting a numerical value "0" when said output of said delay element is at logical "0", and a numerical value "1" when said output of said delay element is at logical "1"; and
    an adder coupled to said counter and said data selector, for adding an output of said data selector to said output of said counter in modulo 2N.

5. A phase detection circuit as claimed in claim 2, wherein said phase inversion correction means includes:

logical product elements coupled to said delay element, for generating logical products of said output of said delay element and respective bits of a numerical value "N"; and
an adder coupled to said counter and said logical product elements, for adding outputs of said logical product elements with said output of said counter in modulo 2N.

6. A phase detection circuit as claimed in claim 2, wherein:

said counter (403a) counts a clock having a frequency practically equal to 2^M times said frequency of said input signal, where M is a positive integer; and
said phase inversion correction means (500a) includes a second exclusive OR element (503) coupled to said output of said delay element (401) and a most significant bit of said output of said counter (403a), said second exclusive OR element (503) generating a logical exclusive OR of said output of said delay element (401) and said most significant bit of said output ofsaid counter (403), wherein an output of said phase inversion corrector means (500a) consists of a combination of least significant bits of said output of said modulo 2N counter (403) and said logical exclusive OR output of said second exclusive OR element (503).

7. A differentialdetection demodulator for demodulating a 2-level quantized received signal using a phase reference signal having a fixed frequency practically equal to a frequency of said received signal, said differential detection demodulator comprising:

half-period detection means (901) for generating, in response to said received signal, a half-period detection signal at each half-period of said received signal;
phase reference signal generation means (902) for generating said phase reference signal in response to a clock having a frequency not less than twice said frequency of said received signal;
phase shift measurement means (903), coupled to said half-period detection means (901) and phase reference signal generation means (902) and including phase inversion correction means (500) for correcting said phase reference signal for a phase inversion thereof at each alternate half-period of said received signal, said phase shift measurement means (903) outputting a relative phase signal representing a relative phase of said received signal with respect to said phase reference signal at each half-period of said received signal, on the basis of said phase reference signal corrected by said phase inversion correction means (500) and said half-period detection signal output from said half-period detection means (901);
a delay element (40) coupled to said phase shift measurement means (903), for delaying said relative phase signal output from said phase shift measurement means (903) by one symbol period of said received signal; and
a subtractor (41) coupled to said phase shift measurement means (903) and said delay element (40), for subtracting an output of said delay element (40) form said relative phase signal.

8. A differential detection demodulator according to claim 7, wherein

said half-period detection means (901) of said phase detection circuit includes: a delay element (401) for delaying said input signal by a delay time shorter than said half-period of said input signal; and a first exclusive OR element (402) for generating a logical exclusive OR of said input signal and an output of said delay element;
said phase reference signal generation means (902) includes a counter (403) for counting in modulo2N a clock having a frequency practically equal to 2N times said frequency of said input signal, where N is a positive integer;
said phase inversion correction means (500) adds a numerical value "0" or "N" in modulo 2N to an output of said counter (403) in response to said output of said delay element (401); and
said phase shift measurement means (903) includes, in addition to said phase inversion correction means (500), a D flip-flop array (404) coupled to said phase inversion correction means (500) and said first exclusive OR element (402), said D flip-flop array (404) holding an output of said phase inversion correction means (500) in response to said logical exclusive OR output of said exclusive OR element (402), wherein a value held in said D flip-flop array (404) constitutes an output of said phase shift measurement means (903).

9. A differential detection demodulator according to claim 7, wherein said phase inversion correction means (500) of said phase detection circuit includes:

a multiplier (501) coupled to said delay element (401), for multiplying said output of said delay element (401) by N; and

an adder (502) coupled to said counter (403) and said multiplier (501), for adding an output of said multiplier (501) to said output of said counter (403) in modulo 2N.

10. A differential detection demodulator according to claim 7, wherein said phase inversion correction means of said phase detection circuit includes:

a data selector coupled to said delay element, for selecting a numerical value "0" when said output of said delay element is at logical "0", and a numerical value "1" when said output of said delay element is at logical "1"; and

an adder coupled to said counter and said data selector, for adding an output of said data selector to said output of said counter in modulo 2N.

11. A differential detection demodulator according to claim 7, wherein said phase inversion correction means of said phase detection circuit includes:

logical product elements coupled to said delay element, for generating logical products of said output of said delay element and respective bits of a numerical value "N"; and

an adder coupled to said counter and said logical product elements, for adding outputs of said logical product elements with said output of said counter in modulo 2N.

12. A differential detection demodulator according to claim 7, wherein:

said counter (403a) counts a clock having a frequency practically equal to 2^M times said frequency of said input signal, where M is a positive integer; and

said phase inversion correction means (500a) includes a second exclusive OR element (503) coupled to said output of said delay element (401) and a most significant bit of said output of said counter (403), said second exclusive OR element (503) generating a logical exclusive OR of said output of said delay element (401) and said most significant bit of said output of said counter (403), wherein an output of said phase inversion correction means (500a) consists of a combination of least significant bits of said output of said modulo 2N counter (403) and said logical exclusive OR output of said second exclusive OR element (503).

13. A method for detecting a phase shift of an input signal relative to a phase reference signal, comprising the steps of:

generating, in response to said input signal, a half-period detection signal at each half-period of said input signal;

generating said phase reference signal in response to a clock having a frequency not less than twice a frequency of said input signal; correcting said phase reference signal for a phase inversion thereof at each alternate half-period of said input signal; and

measuring a phase shift of said input signal with respect to said phase reference signal at each half-period of said input signal, on the basis of said corrected phase reference signal and said half-period detection signal.

FIG. 1

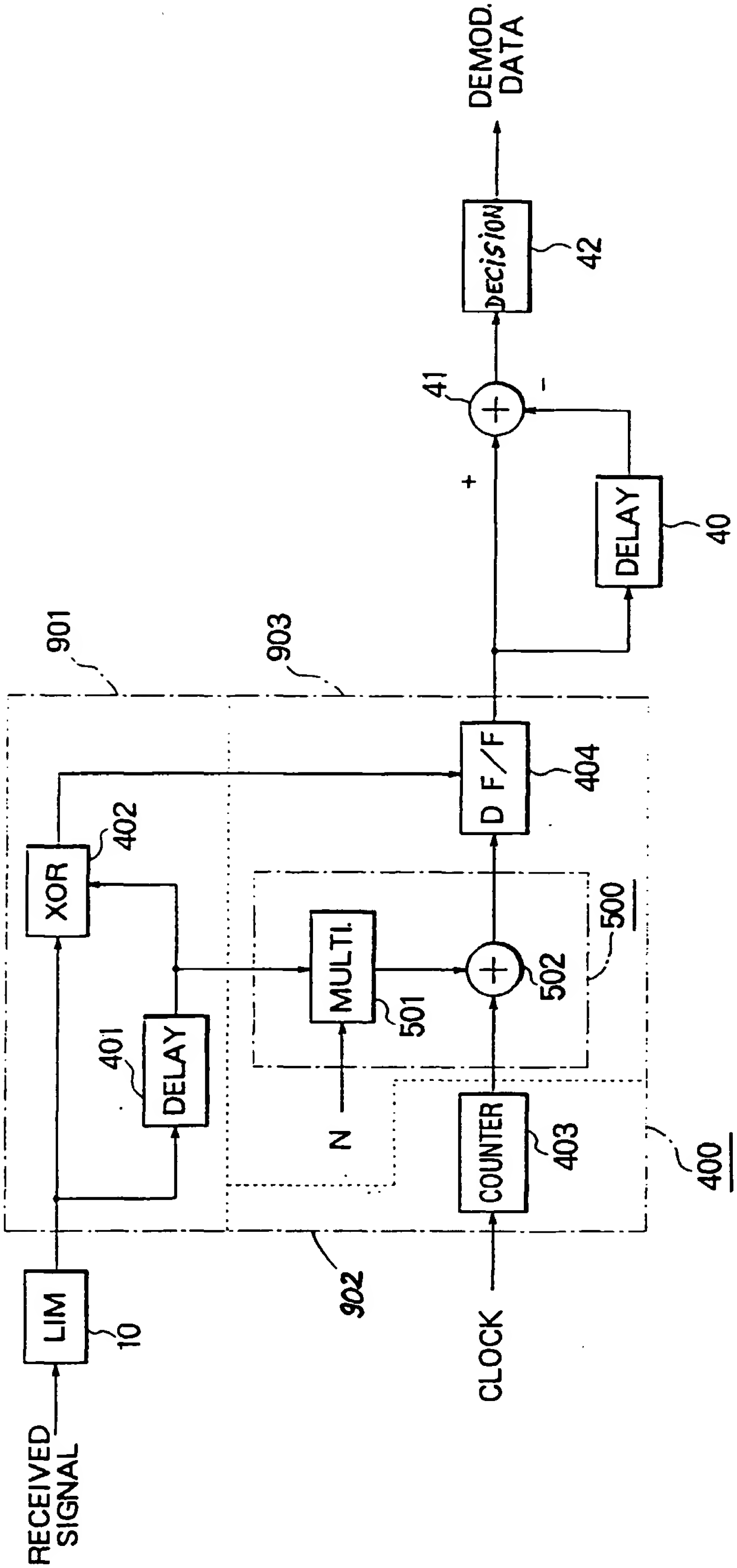

RECEIVED SIGNAL
LIM
10
CLOCK
902
901
903
XOR
402
DELAY
401
MULTI.
501
N
502
500
COUNTER
403
400
D F/F
404
DELAY
40
+
-
41
DECISION
42
DEMOD. DATA

FIG. 2

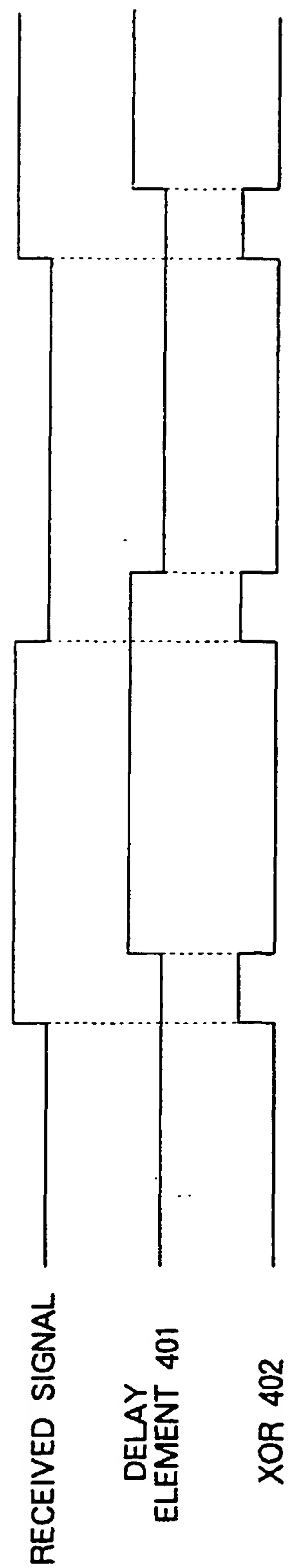


FIG. 3

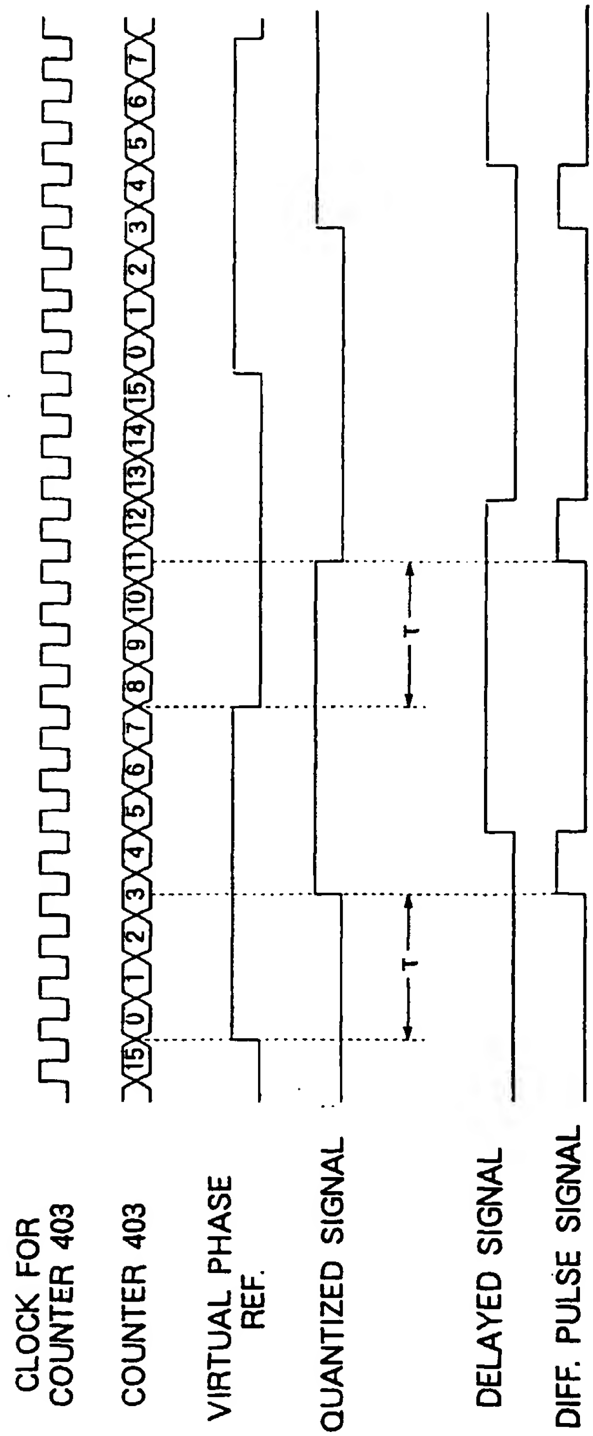

CLOCK FOR COUNTER 403
COUNTER 403
VIRTUAL PHASE REF.
QUANTIZED SIGNAL
DELAYED SIGNAL
DIFF. PULSE SIGNAL
T
T

FIG. 4

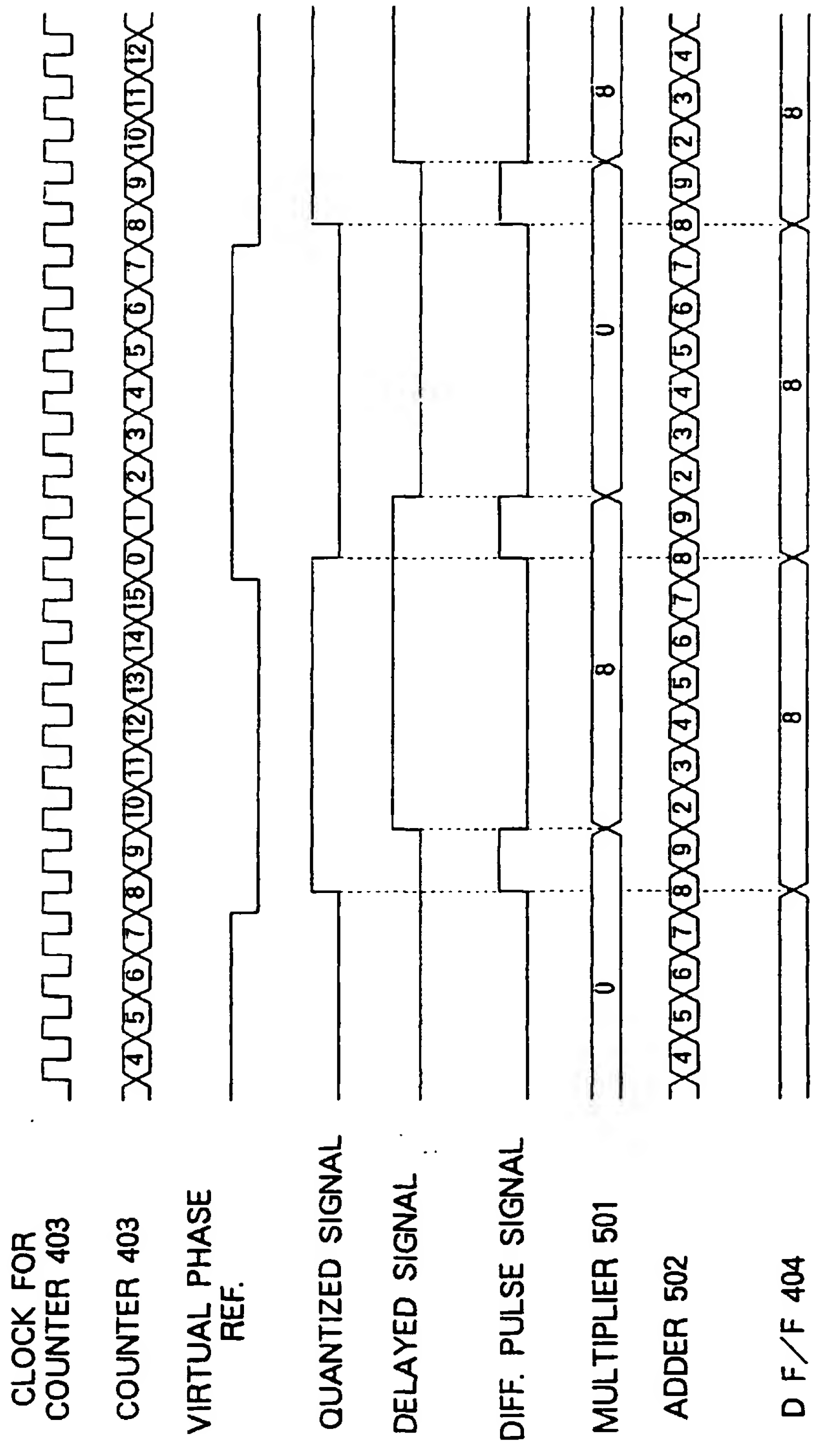

CLOCK FOR COUNTER 403
COUNTER 403
VIRTUAL PHASE REF.
QUANTIZED SIGNAL
DELAYED SIGNAL
DIFF. PULSE SIGNAL
MULTIPLIER 501
ADDER 502
D F/F 404

FIG. 5

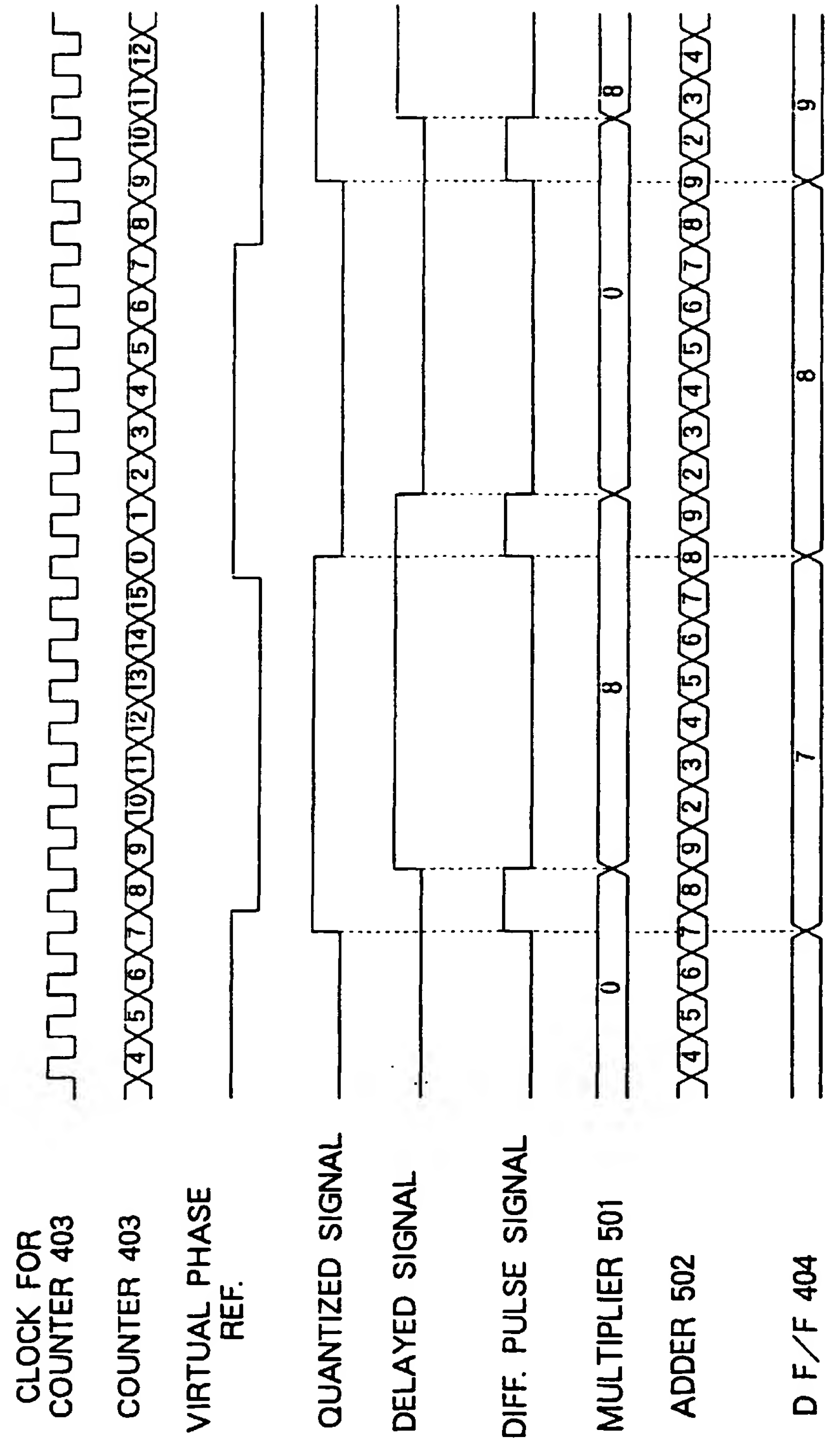

CLOCK FOR COUNTER 403
COUNTER 403
VIRTUAL PHASE REF.
QUANTIZED SIGNAL
DELAYED SIGNAL
DIFF. PULSE SIGNAL
MULTIPLIER 501
ADDER 502
D F/F 404

FIG. 6

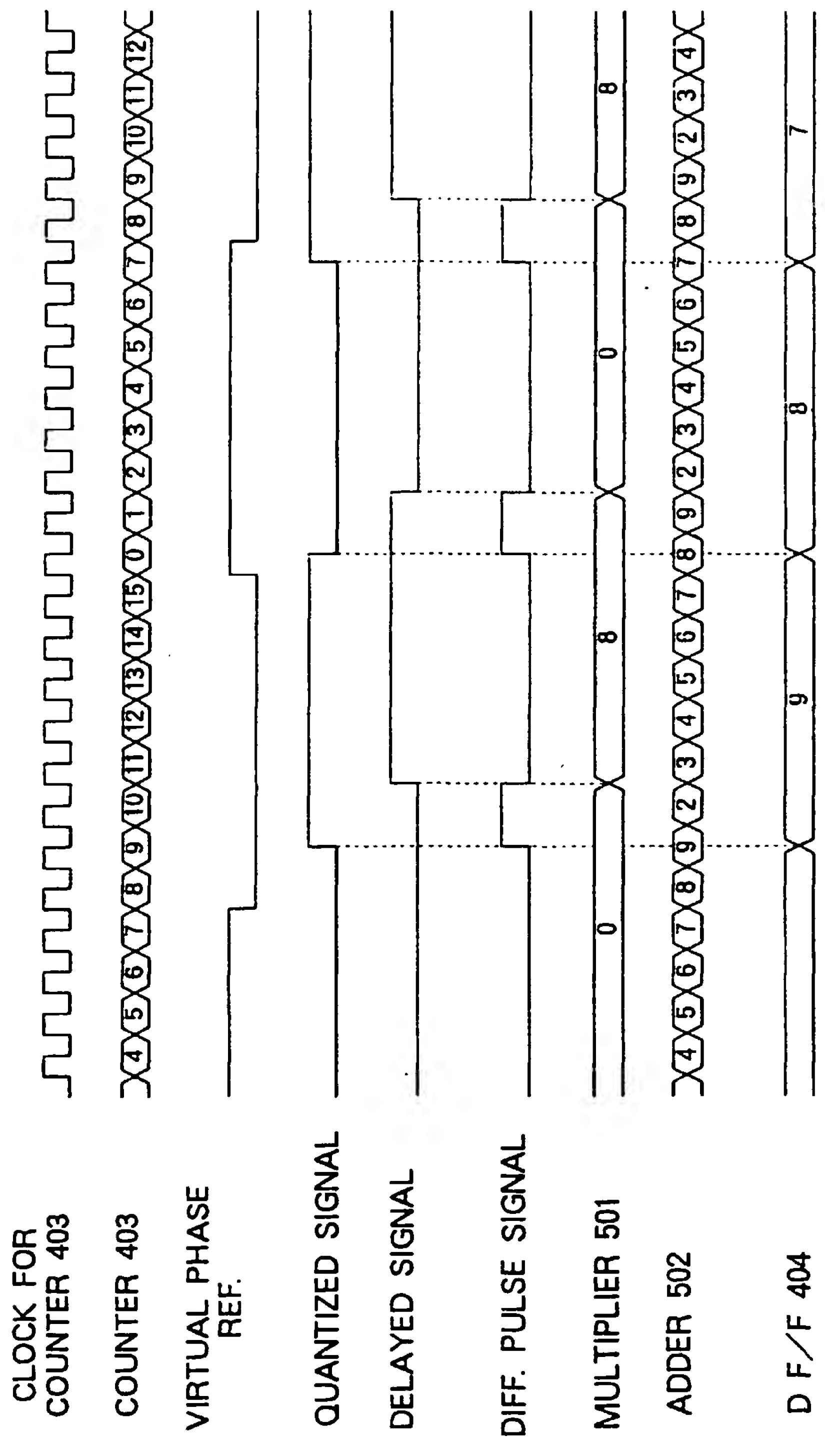
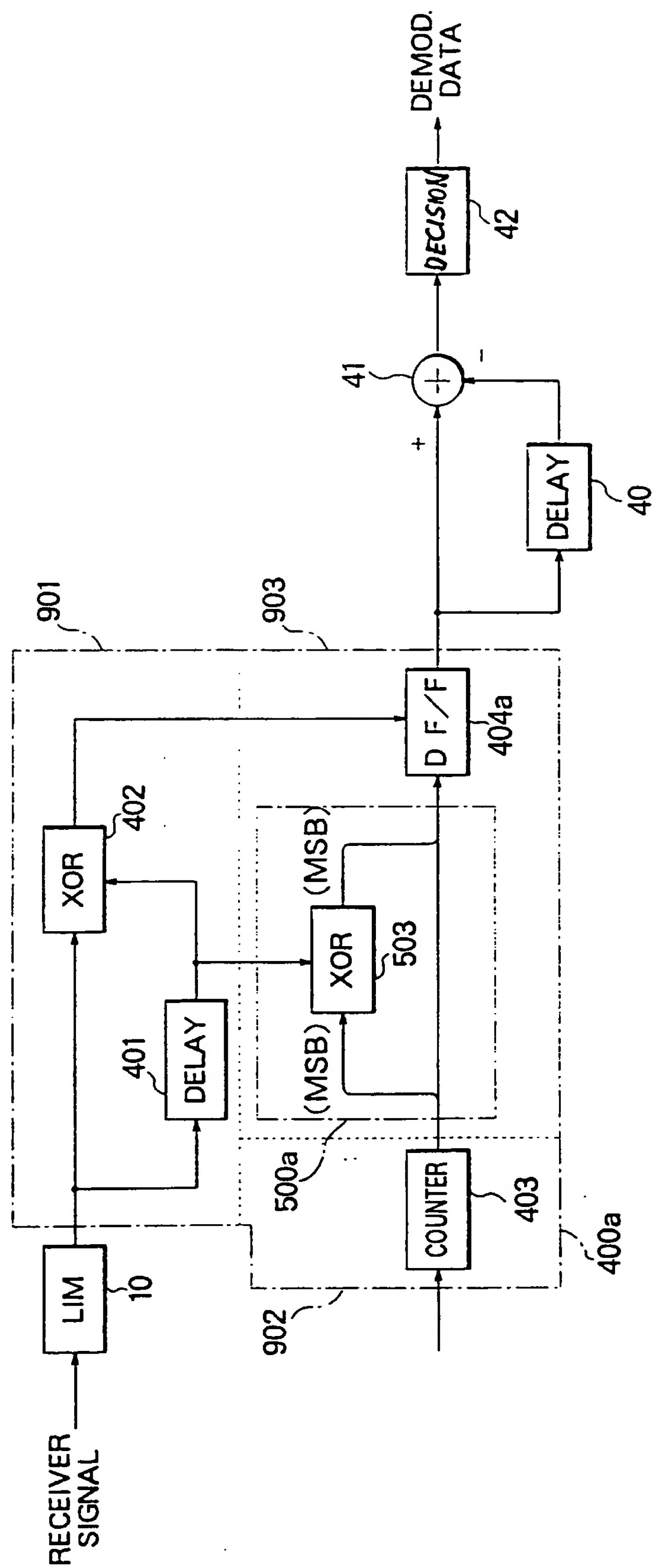

CLOCK FOR COUNTER 403
COUNTER 403
VIRTUAL PHASE REF.
QUANTIZED SIGNAL
DELAYED SIGNAL
DIFF. PULSE SIGNAL
MULTIPLIER 501
ADDER 502
D F/F 404

FIG. 7



RECEIVER SIGNAL
LIM
10
DELAY
401
XOR
402
D F/F
404a
COUNTER
403
XOR
503
(MSB)
(MSB)
500a
400a
901
902
903
DELAY
40
41
+
-
DECISION
42
DEMOD. DATA

FIG. 8

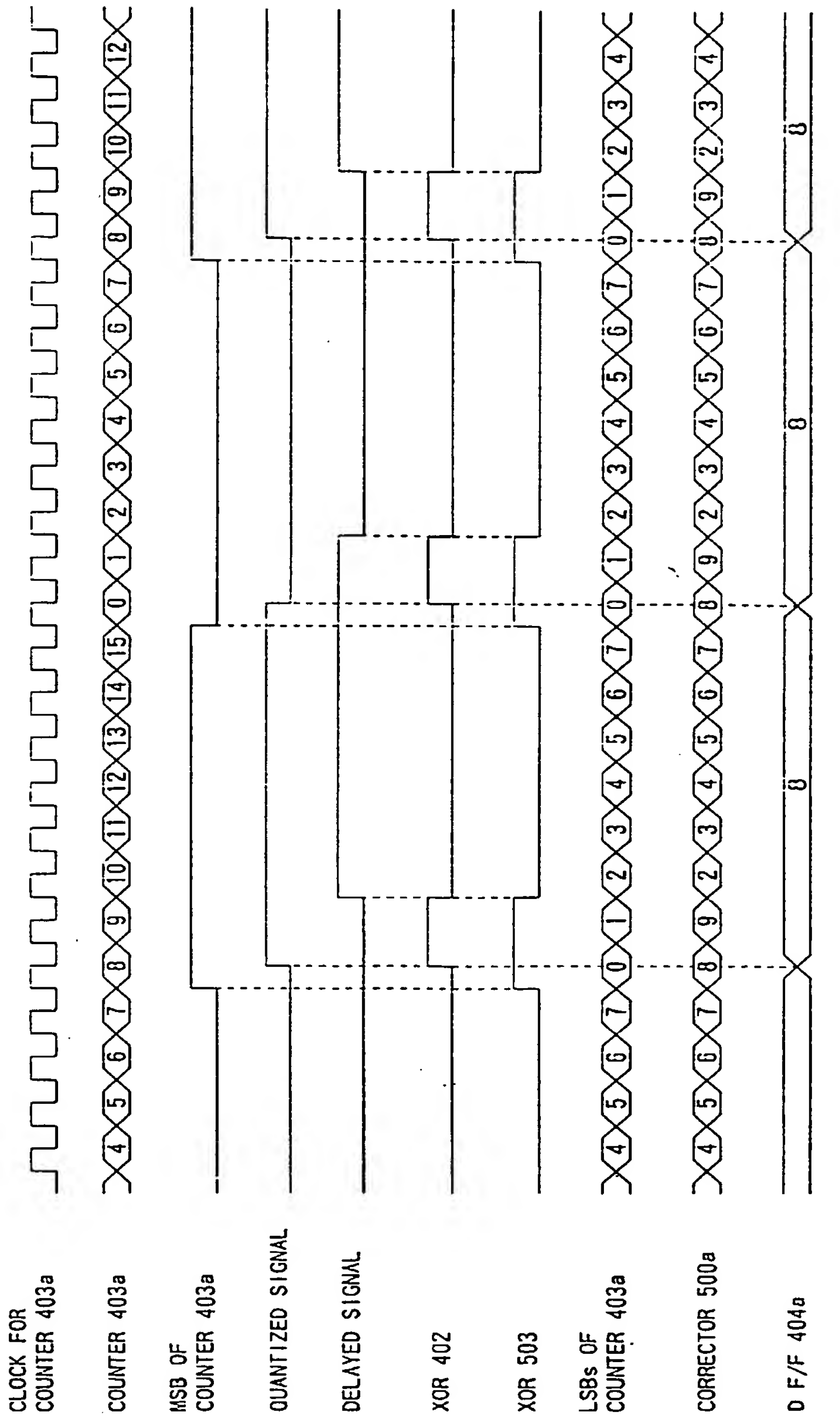

CLOCK FOR COUNTER 403a
COUNTER 403a
MSB OF COUNTER 403a
QUANTIZED SIGNAL
DELAYED SIGNAL
XOR 402
XOR 503
LSBs OF COUNTER 403a
CORRECTOR 500a
D F/F 404a
4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12
4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 0 1 2 3 4
4 5 6 7 8 9 2 3 4 5 6 7 8 9 2 3 4 5 6 7 8 9 2 3 4
8 8 8

FIG. 9

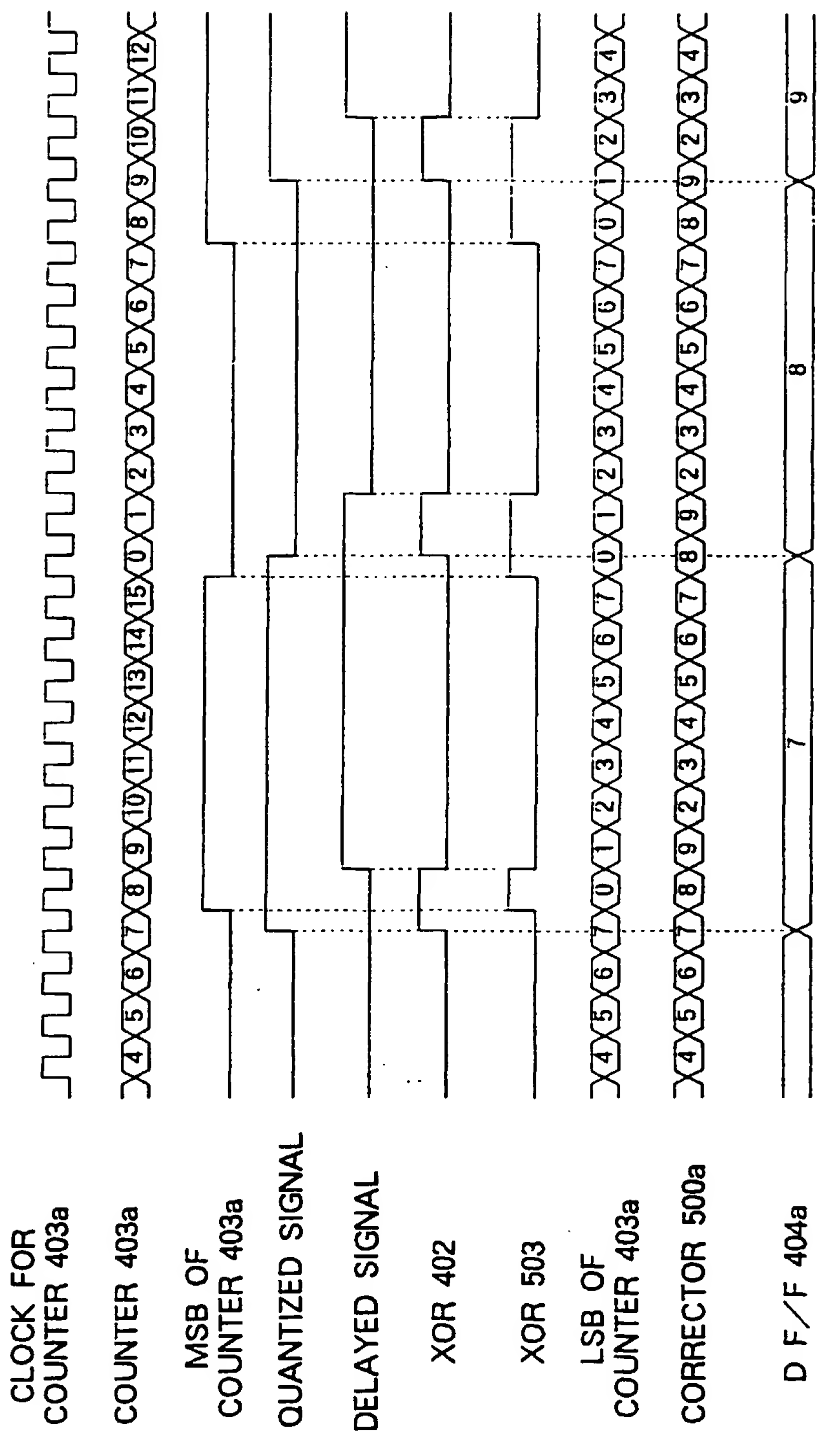

CLOCK FOR COUNTER 403a
COUNTER 403a
MSB OF COUNTER 403a
QUANTIZED SIGNAL
DELAYED SIGNAL
XOR 402
XOR 503
LSB OF COUNTER 403a
CORRECTOR 500a
D F/F 404a

FIG. 10

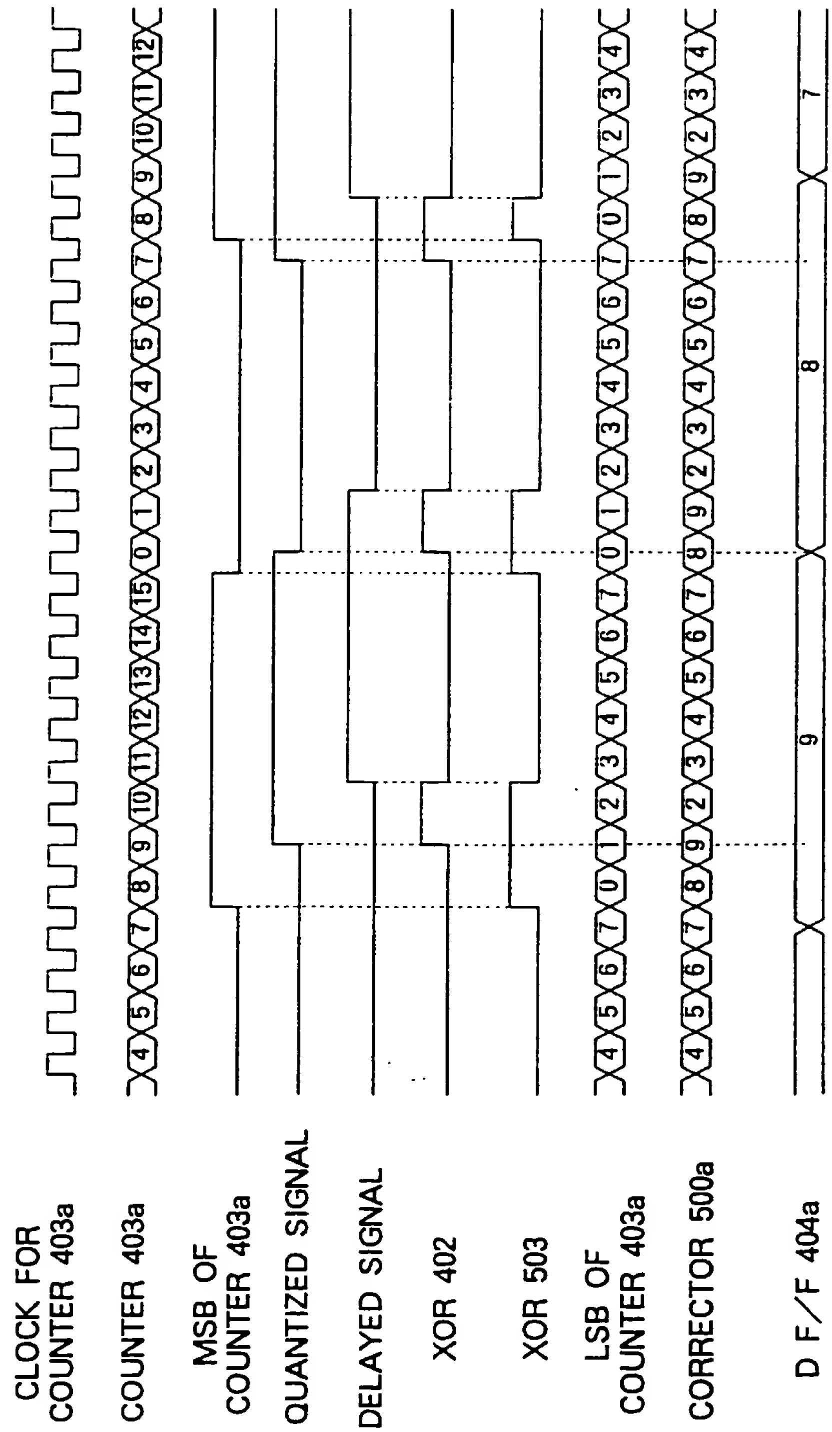

CLOCK FOR COUNTER 403a
COUNTER 403a
MSB OF COUNTER 403a
QUANTIZED SIGNAL
DELAYED SIGNAL
XOR 402
XOR 503
LSB OF COUNTER 403a
CORRECTOR 500a
D F/F 404a

FIG. 11

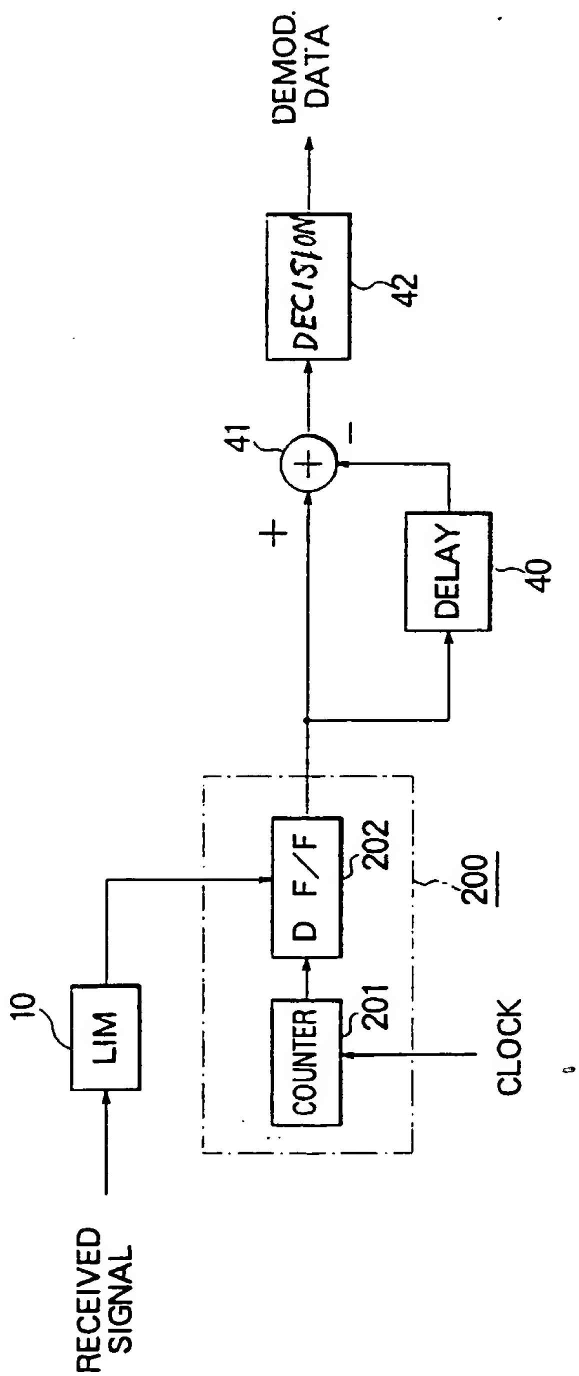

RECEIVED SIGNAL
LIM
10
COUNTER
201
D F/F
202
200
CLOCK
DELAY
40
+
−
41
DECISION
42
DEMOD. DATA

FIG. 12

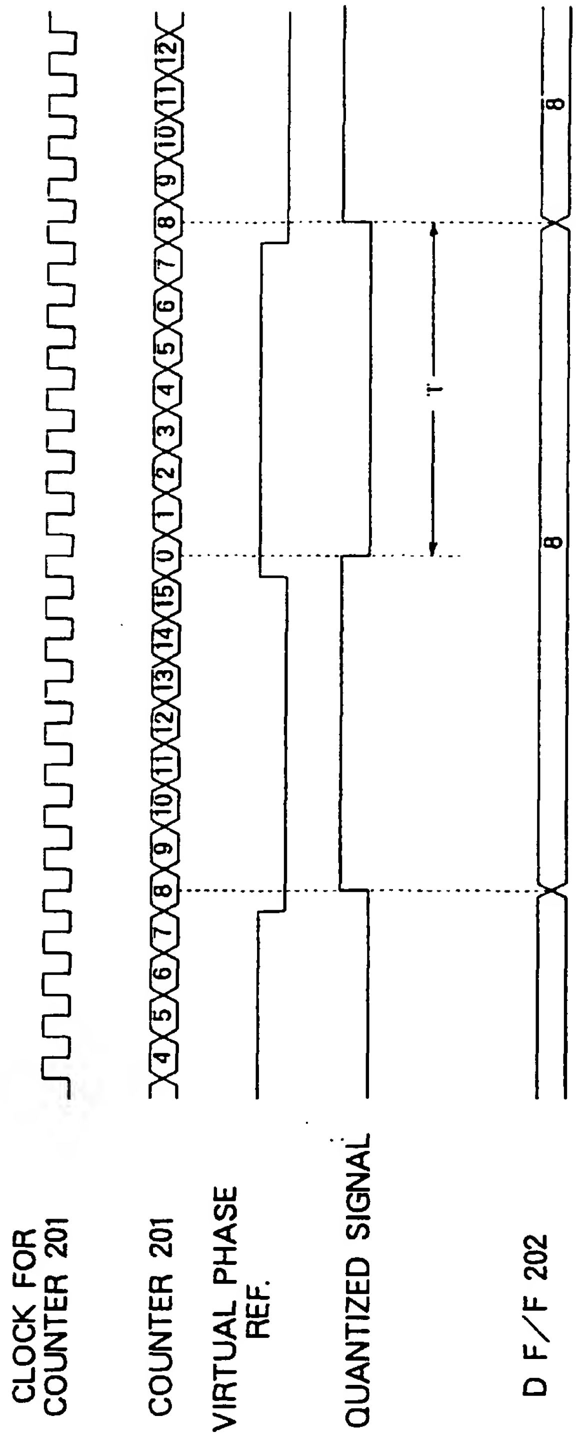
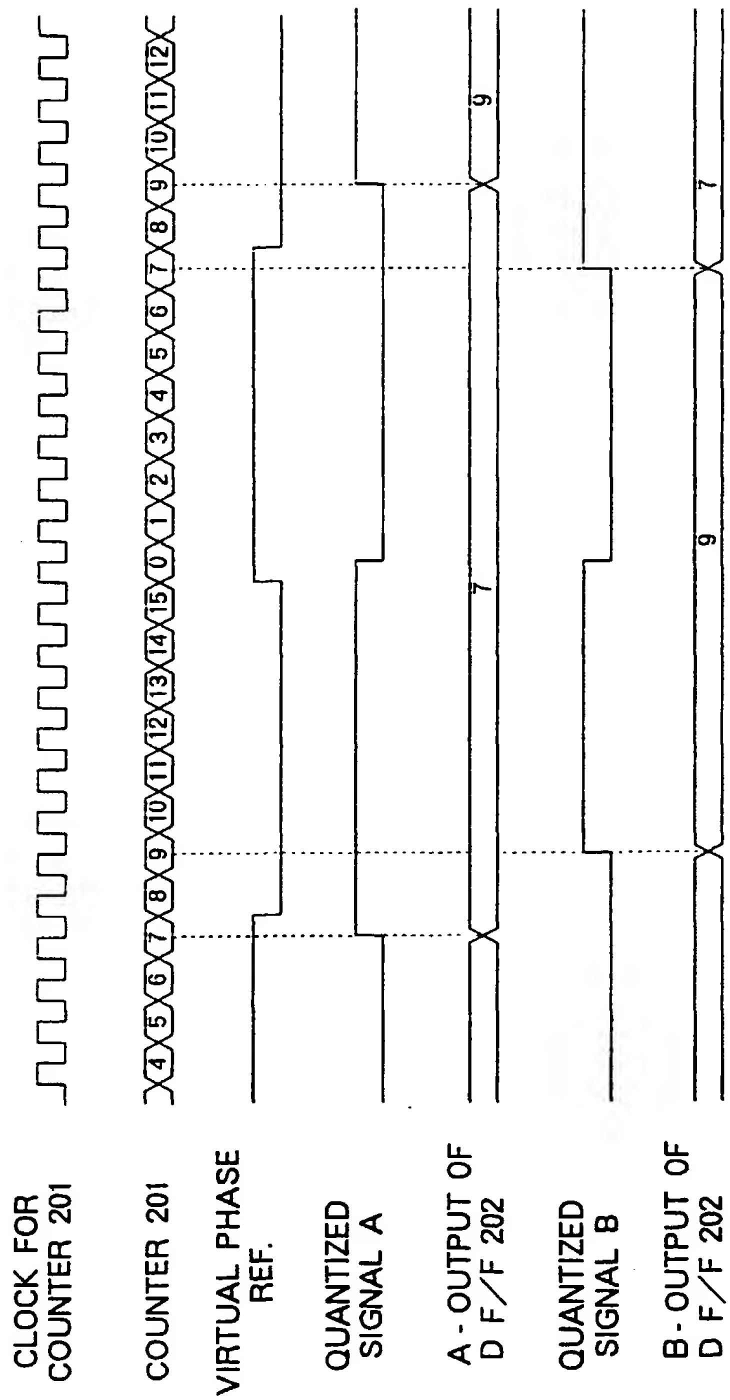

CLOCK FOR COUNTER 201
COUNTER 201
4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12
VIRTUAL PHASE REF.
QUANTIZED SIGNAL
T
D F/F 202
8
8

FIG. 13


CLOCK FOR COUNTER 201
COUNTER 201
4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12
VIRTUAL PHASE REF.
QUANTIZED SIGNAL A
A - OUTPUT OF D F/F 202
7
9
QUANTIZED SIGNAL B
B - OUTPUT OF D F/F 202
9
7